



# DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

The SN54/74LS90, SN54/74LS92 and SN54/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to  $\overline{CP}$ ) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Divide-by-Twelve, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

### PIN NAMES

$\overline{CP}_0$	Clock (Active LOW going edge) Input to +2 Section
$\overline{CP}_1$	Clock (Active LOW going edge) Input to +5 Section (LS90), +6 Section (LS92)
$\overline{CP}_1$	Clock (Active LOW going edge) Input to +8 Section (LS93)
MR <sub>1</sub> , MR <sub>2</sub>	Master Reset (Clear) Inputs
MS <sub>1</sub> , MS <sub>2</sub>	Master Set (Preset-9, LS90) Inputs
Q <sub>0</sub>	Output from +2 Section (Notes b & c)
Q <sub>1</sub> , Q <sub>2</sub> , Q <sub>3</sub>	Outputs from +5 (LS90), +6 (LS92), +8 (LS93) Sections (Note b)

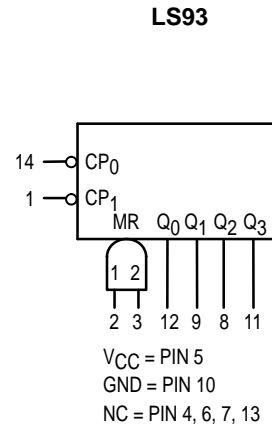
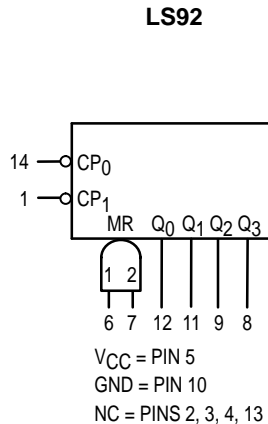
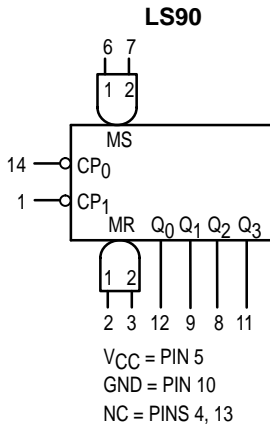
### LOADING (Note a)

	HIGH	LOW
$\overline{CP}_0$	0.5 U.L.	1.5 U.L.
$\overline{CP}_1$	0.5 U.L.	2.0 U.L.
$\overline{CP}_1$	0.5 U.L.	1.0 U.L.
MR <sub>1</sub> , MR <sub>2</sub>	0.5 U.L.	0.25 U.L.
MS <sub>1</sub> , MS <sub>2</sub>	0.5 U.L.	0.25 U.L.
Q <sub>0</sub>	10 U.L.	5 (2.5) U.L.
Q <sub>1</sub> , Q <sub>2</sub> , Q <sub>3</sub>	10 U.L.	5 (2.5) U.L.

### NOTES:

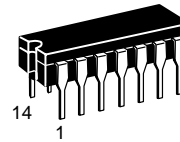
- 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
- The Q<sub>0</sub> Outputs are guaranteed to drive the full fan-out plus the  $\overline{CP}_1$  input of the device.
- To insure proper operation the rise (t<sub>r</sub>) and fall time (t<sub>f</sub>) of the clock must be less than 100 ns.

### LOGIC SYMBOL

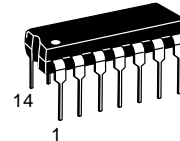


**SN54/74LS90  
SN54/74LS92  
SN54/74LS93**

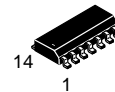
**DECADE COUNTER;  
DIVIDE-BY-TWELVE COUNTER;  
4-BIT BINARY COUNTER  
LOW POWER SCHOTTKY**



**J SUFFIX  
CERAMIC  
CASE 632-08**



**N SUFFIX  
PLASTIC  
CASE 646-06**



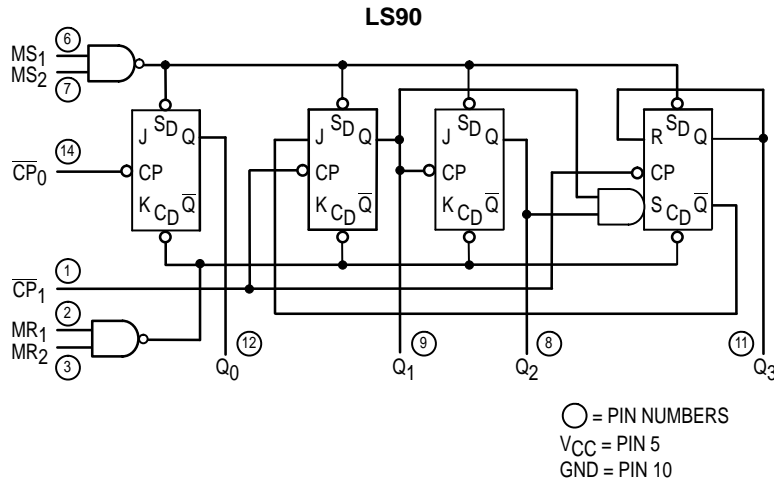
**D SUFFIX  
SOIC  
CASE 751A-02**

### ORDERING INFORMATION

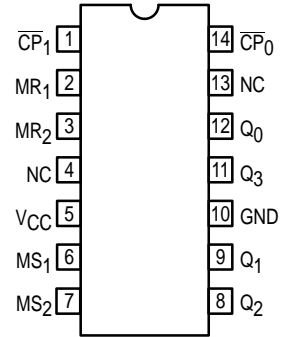
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

# SN54/74LS90 • SN54/74LS92 • SN54/74LS93

## LOGIC DIAGRAM



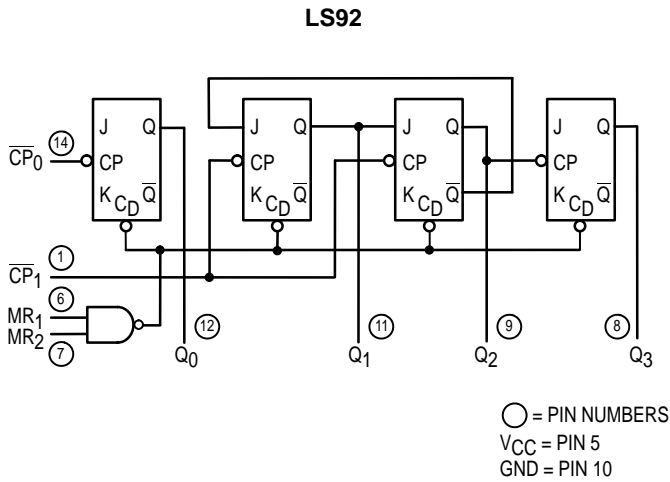
## CONNECTION DIAGRAM DIP (TOP VIEW)



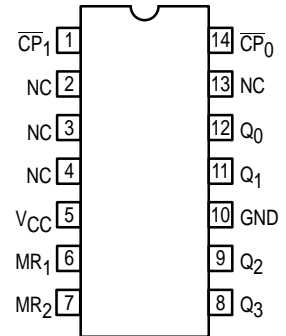
NC = NO INTERNAL CONNECTION

NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

## LOGIC DIAGRAM



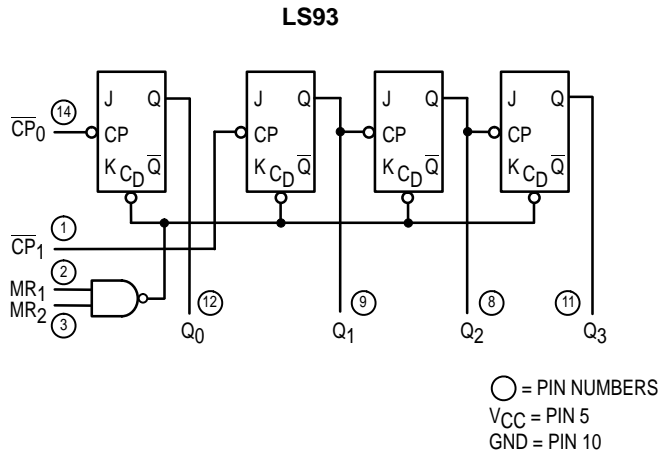
## CONNECTION DIAGRAM DIP (TOP VIEW)



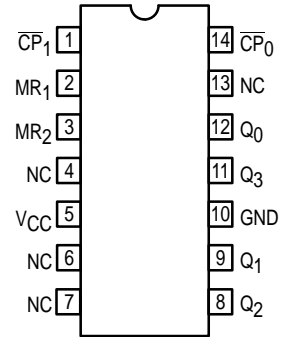
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## LOGIC DIAGRAM



## CONNECTION DIAGRAM DIP (TOP VIEW)



NC = NO INTERNAL CONNECTION

NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

## SN54/74LS90 • SN54/74LS92 • SN54/74LS93

### FUNCTIONAL DESCRIPTION

The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The  $Q_0$  output of each device is designed and specified to drive the rated fan-out plus the  $\overline{CP}_1$  input of the device.

A gated AND asynchronous Master Reset ( $MR_1 \bullet MR_2$ ) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ( $MS_1 \bullet MS_2$ ) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

#### LS90

- A. BCD Decade (8421) Counter — The  $\overline{CP}_1$  input must be externally connected to the  $Q_0$  output. The  $\overline{CP}_0$  input receives the incoming count and a BCD count sequence is produced.
- B. Symmetrical Bi-quinary Divide-By-Ten Counter — The  $Q_3$  output must be externally connected to the  $\overline{CP}_0$  input. The input count is then applied to the  $\overline{CP}_1$  input and a divide-by-ten square wave is obtained at output  $Q_0$ .

- C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ( $\overline{CP}_0$  as the input and  $Q_0$  as the output). The  $\overline{CP}_1$  input is used to obtain binary divide-by-five operation at the  $Q_3$  output.

#### LS92

- A. Modulo 12, Divide-By-Twelve Counter — The  $\overline{CP}_1$  input must be externally connected to the  $Q_0$  output. The  $\overline{CP}_0$  input receives the incoming count and  $Q_3$  produces a symmetrical divide-by-twelve square wave output.
- B. Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The  $\overline{CP}_1$  input is used to obtain divide-by-three operation at the  $Q_1$  and  $Q_2$  outputs and divide-by-six operation at the  $Q_3$  output.

#### LS93

- A. 4-Bit Ripple Counter — The output  $Q_0$  must be externally connected to input  $\overline{CP}_1$ . The input count pulses are applied to input  $\overline{CP}_0$ . Simultaneous divisions of 2, 4, 8, and 16 are performed at the  $Q_0$ ,  $Q_1$ ,  $Q_2$ , and  $Q_3$  outputs as shown in the truth table.
- B. 3-Bit Ripple Counter — The input count pulses are applied to input  $\overline{CP}_1$ . Simultaneous frequency divisions of 2, 4, and 8 are available at the  $Q_1$ ,  $Q_2$ , and  $Q_3$  outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

# SN54/74LS90 • SN54/74LS92 • SN54/74LS93

**LS90  
MODE SELECTION**

RESET/SET INPUTS				OUTPUTS			
MR <sub>1</sub>	MR <sub>2</sub>	MS <sub>1</sub>	MS <sub>2</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X			Count	
X	L	X	L			Count	
L	X	X	L			Count	
X	L	L	X			Count	

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

**LS92 AND LS93  
MODE SELECTION**

RESET INPUTS		OUTPUTS			
MR <sub>1</sub>	MR <sub>2</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
H	H	L	L	L	L
L	H			Count	
H	L			Count	
L	L			Count	

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

**LS90  
BCD COUNT SEQUENCE**

COUNT	OUTPUT			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q<sub>0</sub> is connected to Input CP<sub>1</sub> for BCD count.

**LS92  
TRUTH TABLE**

COUNT	OUTPUT			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

NOTE: Output Q<sub>0</sub> is connected to Input CP<sub>1</sub>.

**LS93  
TRUTH TABLE**

COUNT	OUTPUT			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q<sub>0</sub> is connected to Input CP<sub>1</sub>.

# SN54/74LS90 • SN54/74LS92 • SN54/74LS93

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54 74			4.0 8.0	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.7	3.5	V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current MS, MR CP <sub>0</sub> CP <sub>1</sub> (LS90, LS92) CP <sub>1</sub> (LS93)			-0.4 -2.4 -3.2 -1.6	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current			15	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN54/74LS90 • SN54/74LS92 • SN54/74LS93

AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ ,  $C_L = 15\text{ pF}$ )

Symbol	Parameter	Limits									Unit
		LS90			LS92			LS93			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{MAX}}$	$\overline{\text{CP}}_0$ Input Clock Frequency	32			32			32			MHz
$f_{\text{MAX}}$	$\overline{\text{CP}}_1$ Input Clock Frequency	16			16			16			MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay, $\overline{\text{CP}}_0$ Input to $Q_0$ Output		10 12	16 18		10 12	16 18		10 12	16 18	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	$\overline{\text{CP}}_0$ Input to $Q_3$ Output		32 34	48 50		32 34	48 50		46 46	70 70	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	$\overline{\text{CP}}_1$ Input to $Q_1$ Output		10 14	16 21		10 14	16 21		10 14	16 21	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	$\overline{\text{CP}}_1$ Input to $Q_2$ Output		21 23	32 35		10 14	16 21		21 23	32 35	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	$\overline{\text{CP}}_1$ Input to $Q_3$ Output		21 23	32 35		21 23	32 35		34 34	51 51	ns
$t_{\text{PLH}}$	MS Input to $Q_0$ and $Q_3$ Outputs		20	30							ns
$t_{\text{PHL}}$	MS Input to $Q_1$ and $Q_2$ Outputs		26	40							ns
$t_{\text{PHL}}$	MR Input to Any Output		26	40		26	40		26	40	ns

AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ )

Symbol	Parameter	Limits						Unit
		LS90		LS92		LS93		
		Min	Max	Min	Max	Min	Max	
$t_W$	$\overline{\text{CP}}_0$ Pulse Width	15		15		15		ns
$t_W$	$\overline{\text{CP}}_1$ Pulse Width	30		30		30		ns
$t_W$	MS Pulse Width	15						ns
$t_W$	MR Pulse Width	15		15		15		ns
$t_{\text{rec}}$	Recovery Time MR to $\overline{\text{CP}}$	25		25		25		ns

RECOVERY TIME ( $t_{\text{rec}}$ ) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs

## AC WAVEFORMS

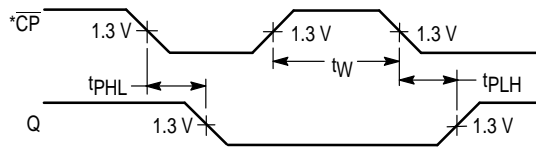


Figure 1

\*The number of Clock Pulses required between the  $t_{\text{PHL}}$  and  $t_{\text{PLH}}$  measurements can be determined from the appropriate Truth Tables.

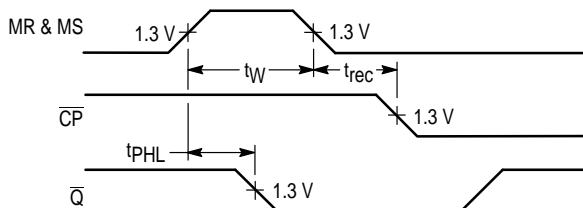


Figure 2

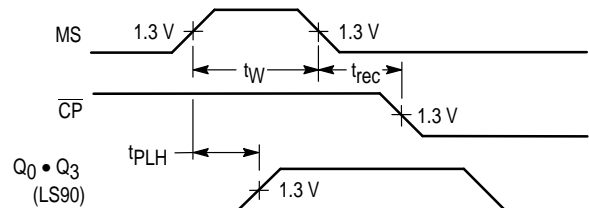


Figure 3